Amendments to the Claims

The following listing of the claims will replace all prior versions, and listings of the claims in the application:

Listing of Claims

1. (Currently Amended) A PLL clock generator for generating an output signal, of which the frequency is N times (where N is a natural number equal to or greater than 1) as high as that of an input signal, the clock generator comprising:

a frequency divider for dividing the frequency of a clock signal by N so as to output a frequency-divided clock signal;

a phase comparator for detecting a phase difference between the input signal and the output signal of the frequency divider so as to output a phase difference signal including information representing the phase difference;

a low pass filter for smoothing the phase difference signal;

a voltage-controlled oscillator for generating the clock signal, of which the frequency is determined by the output of the low pass filter, and outputting the clock signal to the frequency divider; and

a phase shifter for controlling the frequency divider in accordance with the phase difference signal so as to change ~~shifting~~ the phase of the output signal of the frequency divider ~~in accordance with the phase difference signal~~.

2. (Original) The PLL clock generator of claim 1, wherein the phase shifter advances the phase of the output signal of the frequency divider if the phase difference is equal to or smaller than a first value and delays the phase of the output signal of the frequency divider if the phase difference is equal to or greater than a second value.

3. (Original) The PLL clock generator of claim 2, wherein the frequency divider, the phase comparator, the low pass filter and the voltage-controlled oscillator together makes up a first feedback loop, and

wherein the frequency divider, the phase shifter and the phase comparator together make up a second feedback loop.

4. (Currently Amended) A PLL clock generator of claim 1, further ~~for generating an output signal, of which the frequency is N times (where N is a natural number equal to or greater than 1) as high as that of an input signal, the clock generator~~ comprising[[:]]

~~a frequency divider for dividing the frequency of a clock signal by N so as to output a frequency-divided clock signal;~~

~~a phase comparator for detecting a phase difference between the input signal and the output signal of the frequency divider so as to output a phase difference signal including information representing the phase difference;~~

~~a low-pass filter for smoothing the phase difference signal;~~

~~a voltage-controlled oscillator for generating the clock signal, of which the frequency is determined by the output of the low-pass filter, and outputting the clock signal to the frequency divider;~~

~~a phase shifter for shifting the phase of the output signal of the frequency divider in accordance with the phase difference signal; and~~

a synchronization detector for determining a synchronization state of a PLL based on the phase difference signal and for instructing the phase shifter to operate in the case of an asynchronous state.

5. (Original) The PLL clock generator of claim 4, wherein the synchronization detector sums up the absolute values of the phase differences, obtained from the phase comparator, for a predetermined period of time and instructs the phase shifter to start to operate if a resultant summation value is equal to or greater than the predetermined value.

6. (Cancelled)

7. (Original) The PLL clock generator of claim 1, further comprising a binarizer for outputting a binary signal by comparing an incoming analog signal with a predetermined signal level,

wherein the input signal is the binary signal.

8. (Original) The PLL clock generator of claim 4, further comprising a binarizer for outputting a binary signal by comparing an incoming analog signal with a predetermined signal level,

wherein the input signal is the binary signal.

9. (Currently Amended) An optical disc drive for reading and/or writing data from/on an optical disc with wobbled tracks, the optical disc drive comprising:

an optical head for focusing light on one of the tracks and receiving the light that has been reflected from the track;

a wobble signal generator for generating a wobble signal from an output signal of the optical head; and

a ~~the~~ PLL clock generator ~~of claim 7, which receives the wobble signal as the analog signal~~ for receiving the wobble signal and generating an output signal, of which the frequency is N times (where N is a natural number equal to or greater than 1),

wherein the PLL clock generator comprises:

a frequency divider for dividing the frequency of a clock signal by N so as to output a frequency-divided clock signal;

a binarizer for receiving the wobble signal and for outputting a binary signal by comparing the wobble signal with a predetermined signal level,

a phase comparator for receiving the binary signal and detecting a phase difference between the binary signal and the output signal of the frequency divider so as to output a phase difference signal including information representing the phase difference;

a low pass filter for smoothing the phase difference signal;

a voltage-controlled oscillator for generating the clock signal, of which the frequency is determined by the output of the low pass filter, and outputting the clock signal to the frequency divider; and

a phase shifter for controlling the frequency divider in accordance with the phase difference signal so as to change the phase of the output signal of the frequency divider.

10. (Original) The optical disc drive of claim 9, wherein the wobbled tracks of the optical disc are modulated so as to represent address information.

11. (Currently Amended) An optical disc controller ~~including the PLL clock generator of claim 1 and~~ being used for an optical disc drive and including the PLL clock generator for receiving an input signal and for generating an output signal, of which the frequency is N times (where N is a natural number equal to or greater than 1) as high as that of the input signal,

wherein the PLL clock generator comprises:

a frequency divider for dividing the frequency of a clock signal by N so as to output a frequency-divided clock signal;

a phase comparator for receiving the input signal and detecting a phase difference between the input signal and the output signal of the frequency divider so as to output a phase difference signal including information representing the phase difference;

a low pass filter for smoothing the phase difference signal;

a voltage-controlled oscillator for generating the clock signal, of which the frequency is determined by the output of the low pass filter, and outputting the clock signal to the frequency divider; and

a phase shifter for controlling the frequency divider in accordance with the phase difference signal so as to change the phase of the output signal of the frequency divider.

12. (Currently Amended) A method for controlling a PLL clock generator, the PLL clock generator receiving an input signal with a predetermined frequency and generating an output signal, of which the frequency is N times (where N is a natural number equal to or greater than 1) as high as the predetermined frequency,

wherein a first feedback loop is made up with a frequency divider for dividing the frequency of a clock signal by N so as to output a frequency-divided clock signal; a phase comparator for receiving the input signal and detecting a phase difference between the input signal and the output signal of the frequency divider so as to output a phase difference signal including information representing the phase difference; a low pass filter for smoothing the phase difference signal; and a voltage-controlled oscillator for generating the clock signal of

which the frequency is determined by the output of the low pass filter, and outputting the clock signal to the frequency divider;

wherein if the first feedback loop is under an asynchronous state, the method includes the step of controlling the frequency divider based on the phase difference signal and changing the phase of the output signal of the frequency divider.

~~wherein in a loop for controlling the frequency of the output signal in accordance with a phase difference between the input signal and a frequency-divided signal obtained by dividing the frequency of the output signal, if the loop is under the asynchronous state, the method includes the step of changing the phase of the frequency-divided signal.~~

13. (Original) The method of claim 12, wherein if the loop is under the asynchronous state, the method includes the step of performing a feedback control so as to reduce the phase difference by changing the phase of the frequency-divided signal.

14. (New) The PLL clock generator of claim 1, wherein the phase shifter adjusts the number N so as to change the phase of the output signal of the frequency divider.